REMARKS

The above amendments and these remarks are responsive to the Office Action issued on August 31, 2005. By this response, claims 1 and 10 are amended. No new matter is added. Claim 14 was previously cancelled. Claims 1-13 and 15-19 are now active for examination.

The Office Action

The Office Action dated August 31, 2005 rejected claims 1-13 and 15-18 under 35 U.S.C. §103(a) as being unpatentable over Okado (EP 0511484A2) in view of Hennessy (Computer Architecture). Claim 19 stood rejected under 35 U.S.C. §103(a) as being unpatentable over Okado in view of Hennessy and Watanabe (U.S. Patent No. 5,214,786).

It is respectfully submitted that the rejections are overcome in view of the amendments and/or remarks presented herein.

The Obviousness Rejection Based on Okado and Hennessy Is Traversed

Claims 1-13 and 15-18 were rejected as being unpatentable over Okado in view of Hennessy. By this Response, independent claims 1 and 10 are amended. It is respectfully submit that the obviousness rejection is overcome because Okado and Hennessy cannot support a prima facie case of obviousness.

Claim 1, as amended, describes a data processing apparatus comprising an instruction memory in which an instruction is stored, a data memory in which data is stored, and an instruction decoder decoding a fetched instruction. The instruction memory includes a plurality of instruction memory banks. The apparatus further includes a memory operation unit that is coupled to the instruction memory, the data memory and the instruction decoder. The memory operation unit fetches an instruction stored in the instruction memory, and accesses the data

memory according to a decode result of the instruction decoder. An integer operation unit is provided to carry out an integer operation according to a decode result of the instruction decoder. The memory operation unit generates (1) a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle, and (2) a pipeline cycle corresponding to an access to an instruction memory bank **without** any accesses to other instruction memory banks to carry out low power consumption pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks. Therefore, in order to reduce power consumption, an exemplary apparatus of claim 1 provides a specific sequence performing bank selection and bank access, and limits the number of accessed memory banks to reduce power consumption. Specifically, access to a selected memory bank is conducted, while access to an unselected memory bank is **not** performed. Only the required memory bank from a plurality of memory banks is operated according to a result of the bank selection, thereby saves power comparing to conventional memory access in which ALL the memory banks are operated. According to one embodiment of the invention, one memory bank is selected from eight memory banks, and only the selected memory bank is operating.

In contrast, Okado merely describes general memory architecture, and does not teach generating (1) a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle, and (2) a pipeline cycle corresponding to an access to an instruction memory bank **without** any accesses to other instruction memory banks, to carry out low power consumption pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks, as recited in claim 1.

Hennessy, the other cited reference, does not alleviate the deficiencies of Okado. Although the Hennessy reference describes conducting a bank selection process, the selection is performed for

the purpose of data transfer, after the data is read out from the memory banks. Moreover, it is noted that the detailed process involving Hennessy's bank selection is **not** performed in the same way as that described in claim 1. Specifically, the bank selection operation as described in Hennessy does not reduce the number of memory banks that operate during a memory readout process. **Rather**, the Hennessy reference describes a synchronized databank access that performs memory readout in parallel with respect to **all** memory banks. In other words, more than one databank is accessed and in operation at the same time. Since Hennessy always accesses all the banks (memory readout), power consumption cannot be reduced as the apparatus described in claim 1. Consequently, Hennessy fails to disclose "generating...a pipeline cycle corresponding to an access to an instruction memory bank **without any accesses** to other instruction memory banks," as described in claim 1.

Furthermore, according to Hennessy, memory bank accesses (memory readout) are carried out in parallel with respect to all banks. **Then**, a bank selection is conducted to transfer the data that is already read out from the memory banks, in an order depending upon the bank number, subsequent to the memory bank accesses. Therefore, the bank selection is not conducted before bank accesses (memory readout). Accordingly, Hennessy fails to disclose "generating a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle," as described in claim 1.

Thus, Okado and Hennessy, even if combined, do not disclose every limitation of claim 1, and hence cannot support a prima facie case of obviousness. Therefore, the obviousness rejection is untenable and should be withdrawn. Favorable reconsideration of claim 1 is respectfully requested.

Claim 10, like claim 1, describes features relating to generating a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle, and a pipeline cycle corresponding to an access to an instruction memory bank without any accesses to other instruction memory banks to carry out low power consumption pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks. As discussed earlier related to claim 1, neither Okado nor Hennessy discloses these features. Consequently, claim 10 is patentable over the combination of Okado and Hennessy for at least the same reasons as for claim 1. Favorable reconsideration of claim 10 is respectfully requested.

Claims 2-9, 11-13 and 15-18, directly or indirectly, depend on claims 1 and 10, respectively, and incorporate every limitation thereof. Therefore, the obviousness rejection of claims 2-9, 11-13 and 15-18 based on Okado and Hennessy also is untenable and should be withdrawn based on at least the same reasons for claim 1 or 10, as well as based on their own merits. Favorable reconsideration of claims 2-9, 11-13 and 15-18 is respectfully requested.

The Obviousness Rejection Based on Okado, Hennessy and Watanabe Is Overcome

Claim 19 depends on claim 10 and was rejected as being obvious over Okado and Hennessy, and further in view of Watanabe. As pointed out previously, Okado and Hennessy, even if combined, fail to disclose features relating to generating a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle, and a pipeline cycle corresponding to an access to an instruction memory bank without any accesses to other instruction memory banks to carry out low power consumption pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks, as described in claim 10. Watanabe also fails to teach these features. Therefore, Okado, Hennessy and Watanabe, even if

combined, do not teach every limitation of claim 19 by virtue of its dependency from claim 10. Hence, the obviousness rejection based on Okado, Hennessy and Watanabe is untenable and should be withdrawn. Favorable reconsideration of claim 19 is respectfully requested.

For the reasons given above, Applicants believe that this application is conditioned for allowance and Applicants request that the Examiner give the application favorable consideration and permit it to issue as a patent. However, if the Examiner believes that the application can be put in even better condition for allowance, the Examiner is invited to contact Applicants' representatives listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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